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| GRAHAM, ANDREW R | |

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Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/741,912 | MIYASAKA ET AL. | |
| | Examiner | Art Unit | |
| | Andrew Graham | 2644 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 22 December 2000 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. §§ 119 and 120**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Priority*

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

### *Drawings*

2. The drawings are objected to because of following minor informalities:

- In Figure 6, sub-processing blocks (111,121,131) should be relabeled to correctly read, "1st Huffman Decoding Section", "2nd Huffman Decoding Section", and "3rd Huffman Decoding Section", respectively. The inventor of the well-known variable length coding scheme was "Huffman", not "Hoffman" and the word "decording" appears to be a simple typographical error.
- In Figure 12, please change each reference to "Hoffman" to correctly read "Huffman".
- In Figure 17, please change the words "Encording" in component (801) and "Decording" in component (802) to "Encoding" and "Decoding", respectively.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

***Specification***

3. The disclosure is objected to because of the following informality:

The applicant is requested to change all references to "Hoffman" in the specification to "Huffman".

Appropriate correction is required.

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "Parallel Signal Processing Device for a Portable Audio System".

***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. **Claims 9 and 18** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

**Claims 9 and 18** recite the limitation "said first process" in the respective fifth lines of each claim, along with "said second process"

in the respective eleventh and twelfth lines of each claim. There is insufficient antecedent basis for these limitations in the claims.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. **Claim 1-2, 9-11, and 18** are rejected under 35 U.S.C. 102(b) as being anticipated by Hall, Jr (USPN 4351025). Hereafter, "Hall, Jr." will simply be referred to as "Hall".

Hall discloses a parallel digital processor architecture that involves the use of a master central processing unit (MC) and a plurality of parallel elemental computers (ECs) (col. 2, lines 41-60). Figure 1 illustrates the connection of the ECs (3) to the MC (1) and the other various components of the system. The ECs perform arithmetic computations on the data provided to the ECs within a specific time period. It is noted that the 'frame' referred to in this rejection is different in terms of definition from the 'frame time' defined in Hall as being relative to the occurrence of an integration update. The definition of a 'frame' used in this rejection is the period for the execution of one composite cycling or operation of the MC and ECs, or the combined, sequential time of the

MC interrupt and the EC non-integrator interrupt, as is shown in Figure 4. Figure 4 depicts an embodiment of the signal processing wherein the processing time of the ECs is greater than that of the MC, though Hall notes that the two time intervals are adjustable (col. 4, lines 33-35). The ECs are executed simultaneously upon receipt of the non-integrator EC interrupt signal (col. 7, lines 59-62). In view of these operations and circuit arrangements, the ECs read on "first to Nth sub signal processing sections each of which is given (N x t + I)th frame signals" of "a first digital signal framed for each predetermined time interval" as well as "each of which completes a first process within a period (N x T)". The MC controls the data transfer among the ECs and also performs logic operations, and again, as depicted in Figure 4, performs a function for a period less than that used by the ECs (col. 1, lines 64-68 and col. 2, lines 1-5). This reads on "a main signal processing section which converts a signal processed in said (i + 1)th sub signal processing section into a second digital signal by completing a second process within a period T".

Regarding **Claim 2**, the data, as it is being processed, is transferred between ECs at the control of the MC (col. 7, lines 53-57). The data is passed along the MC bus (4) shown in Figure 1, and the connections within the EC (3) are shown in more detail in Figure 2. Figure 2 illustrates the connection of MC/EC registers between the MC data and address busses (4,6) and EC data and address buses. The EC data and address buses are connected to the EC CPU (col. 7, lines

5-10). The EC buses that enable the transfer of data from the registers to the EC CPU (18) reads on "a distribution section inputting said first digital signal to one of said first to Nth sub signal processing sections for each frame interval one after another". The circuitry of the MC buses that routes the output of the registers to the MC data bus for redistribution or other processing reads on "a selection section selectively outputting one of the after process signal outputted from said first to Nth sub signal processing sections for each frame interval one after another to input the signal to said main signal processing section".

Regarding **Claim 9**, please refer to the like teachings of Claim 1, particularly the conversion of an input signal to a processed output signal, the latter being prepared to become the input signal for the next stage of processing.

Regarding **Claim 10**, please refer to the like teachings of Claim 1, noting the cyclical processing and handling of the data by the MC and ECs. Regarding **Claim 11**, please refer to the like teachings of Claim 2.

Regarding **Claim 18**, please refer to the like teachings of Claim 10.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. **Claims 1, 2, 8-11, 13, and 17-18** are rejected under 35 U.S.C. 103(a) as being unpatentable over by Ahamed et al (USPN 5978831).

Ahamed discloses a multiprocessor architecture that utilizes processors with different processing rates. As is generally shown in Figure 1, the teachings of Ahamed center around multiple processors connected in parallel, wherein the processing rates of the involved processors are integer multiples of each others and are less than the rate at which data is received in the processing section (col. 7, lines col. 8, lines 66-67 and col. 9, lines 1-3). The basic embodiment shown in Figure 1 uses an input gate (17), buffers (19,20), and an output gate (18) to control the transfer of data between the processors and in and out of the processing section (col. 7, lines 54-67 and col. 8, lines 1-21). With a delay between the input of a particular frame of information data and the output of the same data from the parallel processing scheme, the stage is able to obtain a constant rate of throughput equivalent to the arrival time of the

blocks of information data (col. 7, lines 49-51). The delay of the system is equivalent to the execution period of the slowest processor in the system. Ahamed also discloses that the parallel processing scheme may be implemented into a pipeline wherein the individual parallel processing schemes illustrated in the disclosure are the stages of the pipeline. Ahamed discloses that the stages require the same amount of execution time so that each stage is continually busy (col. 11, lines 31-37). The overall system reads on "A signal processing device" and a single stage of multiple, parallel processors reads on "first to Nth sub signal processing sections each of which is given *N x t + I)th frame signals (I and t are integers, N is a natural number, and $0 \leq i \leq N$) of a first digital signal framed for each predetermined time interval". The execution periods of the multiple processors in parallel reads on "completes a first process within a period (N x T)".

Again, while Ahamed discloses the arrangement of stages of processing in a pipeline, Ahamed does not explicitly teach:

- a main, single processor for performing a function in the processing scheme
- that the single processor completes a process within a period T

However, Ahamed specifically discloses that the multiprocessor stages have an equal functional performance capability to that of a single processor, an equivalence which supports interchangeability (col. 2, lines 47-52). Regarding Figure 14, Ahamed also notes that

any arbitrary segment of the shown pipeline may be replaced by a series processor arrangement, which also suggests the use of a processor with a single input and output as part of the pipelined system (col. 11, lines 51-54 and col. 12, lines 25-28). This second potential stage and form of processing reads on "a main signal processing section which converts a signal processed in said (i+1)th sub signal processing section into a second digital signal". Again, Ahamed discloses that each stage of the pipeline would need the same execution time (col. 11, lines 31-37). With a single processor serving as a stage in the pipeline, this requirement makes obvious that the execution time of the single processor would need to be less than that of the multiple processors in parallel. This aspect of the teachings of Ahamed reads on "completing a second process within a period T".

To one of ordinary skill in the art at the time the invention was made, it would have been obvious to include a single processor as a stage of the pipelined processor architecture of the invention of Ahamed. The motivation behind such a modification would have been the lower price, in certain situations, of using a single processor instead of several. The use of a single processor in a pipeline stage would have also provided the benefits of simpler input, output, and power connections for the particular stage, a reduced physical area required for the stage, as well as only one processing rate to influence the operating clock of the system, as opposed to the

potential multiple clock cycles needed to be addressed in the multiprocessor stages.

Regarding **Claim 2**, the input gate (17) and the input buffer (19) of the first shown embodiment deliver the appropriate blocks of input signal to the appropriate signal processors (col. 7, lines 64-67 and col. 8, lines 1-8). The delivery timing of said input gating component (17) can be seen in Figure 2. These components read on "a distribution section inputting said first digital signal to one of said first to Nth sub signal processing sections for each time frame interval one after another". The output gate (18) outputs the data block in the order of their input (col. 8, lines 8-15). Ahamed also notes that the output gate of one stage may be the input gate of another stage (col. 12, lines 59-62). This output gate (18) reads on "a selection section selectively outputting one of the after-process signal outputted from said first to Nth sub signal processing sections for each frame interval one after another to input the signal to said main signal processing section".

Regarding **Claim 4**, Ahamed does not detail the functions being performed in the stages of the pipeline, but notes the general concept of having different processors with different functionalities incorporated into the same system (col. 4, lines 48-64). The processing blocks are suggestedly separated according to function, but organized sequentially according to process timing (col. 4, lines 60-64). Figure 2 illustrates that the processes performed by the two different processors in the shown embodiment do not require the

sharing or interrelationship of the data that they are respectively processing. This concept generally applies to all functions which can be successfully performed with parallel processors. This reads on "said first process excludes a process employing information generated in the past time frame". Regarding the proposed structure of Claim 1, specifically the stage including a single processor executing a function alone, to meet the throughput required in column 11, lines 31-34, the processor would need to have a processing time equivalent to the time period allowed for each stage. This concept of processing data sequentially reads on "the second process contains a process employing information generated in the past time frame".

Regarding **Claim 8**, Ahamed discloses the use of m parallel processors with any integer relationship between the processing rates of the involved processors (col. 9, lines 1-3). Figure 2 clearly illustrates that the delay time for the parallel stage is equal to the longest processing time, and the collective processors are able to provide output data at the same rate of the reception of the data. To maintain a constant throughput of a period t, it is obvious that each of m processors in a parallel stage would need to perform at least $1/m^{th}$ of the execution per period (t). In other words, under the combination of processors possible as proposed by Ahamed, it is obvious that the maximum potential processing time that can be taken by an individual processor while maintaining a throughput of (t) is equal to m*t if m processors are each outputting one processed data bit per period t. Ahamed, again, also discloses that each stage is

given that same processing time, and thus, where a single processor makes up a stage of the pipeline, the processing time allowed for the single processor is t (col. 11, lines 31-37). These relationships in view of the possible combinations of processors of Ahamed read on "division is made for said first process and said second process so that the calculation period necessary for said first process is N times the calculation period necessary for said second process".

Regarding **Claim 9**, please refer to the like teachings of Claim 1. Regarding **Claim 10**, please refer to the like teachings of Claim 1, noting the possible combinations noted by Ahamed for the different stages of the pipeline. Regarding **Claim 11**, please refer to the like teachings of Claim 2. Regarding **Claim 13**, please refer to the like teachings of Claim 4, and the nature of signals processed in parallel and in series. Regarding **Claim 17**, please refer to the like teachings of Claim 8. Regarding **Claim 18**, please refer to the like teachings of Claim 1 and 10.

8. **Claims 3 and 12** are rejected under 35 U.S.C. 103 (a) as being unpatentable over Ahamed as applied above, and in further view of Matt et al (USPN 6581153). Hereafter, "Matt et al" will simply be referred to as "Matt".

As detailed above, Ahamed discloses a pipelined processor architecture that includes stages with various numbers of processors. Ahamed also discloses the components necessary for properly transferring the data between the processor or processors that make up

each stage of the pipeline, including those that act as both the output for one stage and the input for the next stage. Ahamed discloses the concept of stages of the pipeline having input and output buffers (col. 8, lines 1-15). Ahamed also discloses the use of Input/Output (I/O) buffering, which involves the handling and temporary storing of pre- and post-processed data (col. 6, lines 23-27). These teachings, in view of the processing performed on the respective signals, reads on "a first memory storing said frame signal one after another" and "a second memory storing said frame signal of said second digital signal one after another".

While Ahamed discloses different components for the distribution and selection of the data being received and transferred from the processors in the system, Ahamed does not specify:

- a distribution and selection for controlling data transfer between processing sections
- the connection of a main signal processing section to the two memories, including the respective data transfers between the memories and the main processor

Matt discloses a central router component that handles the transfer of data between a main, single processor and a plurality of individual, function specific processing modules. The router (ROUTER) specifically coordinates the relaying of data between the processing modules (M1,M2,M3) and the main processor (DSP), as well as between the processors and a memory (RAM) (col. 4, lines 13-29). The data for the modules is transferred from the DSP, and the processed data is

then transferred back to the DSP. The RAM can be used to store data before processing by the modules as well as storing data before it's transferred back to the DSP (col. 4, lines 24-52 and col. 6, lines 47-51). The router and its application reads on "a distribution and selection section" and "wherein said first to Nth sub signal processing sections are connected to said distribution and selection section" and "sends the after process signal to said distribution and selection section". The connection of the DSP to input and output paths as seen in Figure 1, in view of the I/O buffering disclosed by Ahamed, reads on "said main signal processing section is connected to said first and second memories" and "picks out said frame signal from said first memory for each time interval T to output said frame signal to said distribution and selection section" and the other relative connections between the memories and the DSP.

To one of ordinary skill in the art at the time the invention was made, it would have been obvious to utilize the central router of Matt to distribute the data between the processing stages of the system of Ahamed. The motivation behind such a modification would have been that the central router would have maintained the processing capabilities of the involved processors while still enabling a single processor to maintain general control of the operation of the overall system. In view of the teachings of Ahamed, the central data router of Matt would have also enabled the same processors to execute different stages of the pipeline.

Regarding **Claim 12**, please refer to the like teachings of Claim 3.

9. **Claims 5-7 and 14-16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahamed as applied above, and in further view of the applicant's admitted prior art.

As detailed above, Ahamed discloses a pipelined processor architecture that includes stages with various numbers of processors. Ahamed also notes the general concept of having different processors with different functionalities incorporated into the same system (col. 4, lines 48-64). The processing blocks are suggestedly separated according to function, but organized sequentially according to processing time (col. 4, lines 60-64).

Ahamed does not disclose particular further details about the functions performed by the different stages of the presented pipeline arrangement, including:

- that the first digital signal is a compressed and encoded signal
- that the second digital signal is a pulse code modulated signal of an audio signal
- that the first process involves converting the information in the data into the frequency spectrum
- that the second process converts the frequency spectrum signal into a time based pulse code modulated signal

However, the applicant has noted that a number of types of compressing/decoding process techniques are known in the art (page 1, lines 9-15 of the submitted specification). Listed processes include subband encoding, MDCT, quantization, and Huffman encoding, as well as the compression technique of MPEG-1 Layer 3. The MPEG-1 Layer 3 encoders are known in the art to include each of these four processes. The Pohlmann reference has been included with this action to provide support for such a position. Figure 11-20-B of Pohlmann clearly illustrates the conversion of an encoded audio bitstream to a stereophonic digital audio signal with an MPEG-1 Layer 3 decoder. In view of this decoding process, as cited as known in the art by applicant, the input signal to the decoder reads on "said first digital signal is a compressed and encoded signal of an audio signal". The output signal of the MPEG-1 Layer 3 decoder reads on "said second digital signal is a PCM signal of an audio signal". The Huffman decoding and bit reallocation of an MPEG-1 Layer 3 decoder reads on "contains a process picking out information from the compressed and encoded signal to convert the information into information of a frequency spectrum". The inverse MDCT procedure and inverse subband filtering of a MPEG-1 Layer 3 decoder reads on "contains a process converting said information of said frequency spectrum into said PCM signal of time base".

To one of ordinary skill in the art at the time the invention was made, it would have been obvious to utilize the processing architecture of Ahamed to perform the audio encoding and decoding

processes noted in the applicant's admitted prior art. The motivation behind such a modification would have been the reliable throughput that the system of Ahamed would have provided for the processes of audio encoding and decoding, processes which heavily rely on the timely presentation and execution of data. Ahamed also discloses that the parallel processing scheme is, in certain instances, more cost effective than a single processor.

Regarding **Claim 6**, the applicant discloses Huffman coding and MDCT as well-known processes in the art. The MPEG-1 Layer 3 decoder and other digital decompression/decoding techniques are well known in the art to include both a Huffman decoder and an inverse MDCT, which reads on "said first process contains a decoding process of a variable length code" and "said second process contains an inverse MDCT process".

Regarding **Claim 7**, the applicant discloses quantization and subband encoding as well-known processes in the art. The MPEG-1 Layer 3 decoder and other digital decompression/decoding techniques are well known in the art to include both an inverse quantizers and sub-band filters, which reads on "said first process contains an inverse quantizing process" and "said second process contains a sub-band synthesis filter bank process".

Regarding **Claim** 14, please refer to the like teachings of Claim 5. Regarding **Claim 15**, please refer to the like teachings of Claim 6. Regarding **Claim 16**, please refer to the like teachings of Claim 7.

10. **Claims 19 and 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahamed as applied above, and in further view of well-known prior art.

As detailed above, Ahamed discloses a pipelined processor architecture that includes stages with various numbers of processors. Ahamed's disclosure focuses on the architecture of the involved processors, not necessarily the large scale device in which said teachings may be implemented. In terms of processing though, please refer to Claim 1 regarding Ahamed's teachings and the "first to Nth sub signal processing sections" and "main signal processing section" in Claim 19.

Ahamed does not specify:

- that the overall device is a portable type apparatus including:
  - an audio signal input section for inputting an encoded audio signal
  - a signal processing device for decoding said audio signal through the use of sub signal processing sections and a main signal processing section

Buchheim discloses a digital music player that is capable of conducting various forms of input and output. The overall player, as shown in Figure 2, the overall device is implemented in a housing shaped like and is the same size as a standard audio cassette, which means that the overall device reads on "A portable type apparatus". The device is able to output a signal through a standard audio

cassette player, built-in speakers, or external speakers (col. 6, lines 1-21). These output paths and devices read on "an audio signal output section for outputting said decoded audio signal". The device is able to receive various, compressed digital audio files through a communicator (34) which connects the device to a computer (36) (col. 7, lines 1-35). This communicator (34) reads on "an audio signal input section for inputting an encoded audio signal". The device also includes an audio chip for encoding and decoding a variety of file formats, which reads on "a signal processing device for decoding said encoded audio signal" (col. 5, lines 42-51).

To one of ordinary skill in the art at the time the invention was made, it would have been obvious to implement the processing scheme of Ahamed into the portable digital audio player of Buchheim. The motivation behind such a modification would have been that the processing structure of Ahamed would have enabled different processors to be implemented in the player at a lower price than a single processor, without a decrease in the throughput of the system.

Regarding **Claim 20**, please refer to the like teachings of Claims 1, 2, and 19, noting that the microphone input ports and encoding capabilities of the device of Buchheim, as well as the memory (16) included in the portable audio player (col. 5, lines 54-56 of Buchheim).

***Conclusion***

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Monroe et al (USPN 5911082) discloses a system that involves a central microprocessor unit and various grades of parallel digital signal processors.

Asano et al (USPN 5237686) discloses an encoding and decoding architecture and system that employs multiple processors operating in parallel.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew Graham whose telephone number is (703) 308-6729. The examiner can normally be reached on Monday-Friday (8:30-5:00). If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Isen, can be reached at (703) 305-4386. The fax number for the organization where this application or proceeding is assigned is 703-872-9314.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Andrew Graham
Examiner
A.U. 2644

ag
January 21, 2004

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SUPERVISORY PATENT EXAMINER
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